Listing of Claims:

Claims 1-33 (canceled)

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9/28/04

34. (currently amended) A bond pad structure, comprising:

a semiconductor substrate;

~~a plurality of conductive bond pads,~~ comprising interlocking grid structures, formed over said semiconductor substrate;

a passivating layer formed over said ~~bond pads~~, interlocking grid structures, having multiple openings to ~~each~~ said interlocking grid structures ~~bond pads~~;

a barrier layer formed over said passivating layer and in said openings;

a conducting pad formed over ~~each~~ said ~~bond pad~~ interlocking grid structures and over said barrier layer, whereby an upper surface of said conductive pad provides improved adhesion for subsequently formed *bonds*.

35. (currently amended) The bond pad structure of Claim 34, wherein said conductive bond ~~pads are~~ pad is formed of copper.

Amendment to the Specification:

(p. 19, last paragraph)

Referring again, in more detail to Fig. 1, a method and structure (in the fabrication of metal pad structures) is shown wherein a unique interlocking grid structure is formed. These interlocking structures form "islands" of interlocking "grid" structures (in three dimensions) to enhance adhesion among the various layer of the metal stack pad structure for improved wire bond strength. The method and structure of said interlocking grid structure 6 is formed by the patterning and etching of passivation material 4, e.g., insulating silicon oxide, silicon nitride, polyimide material, etc.. The said interlocking grid structure 6 is formed of patterned, passivating material 4 in a pad via contact region is , approximately 100 by 100 microns square and the size of the "island" structures are from about 10 to 25 microns in width, approximately 4 microns in height, and from about 4 to 10 in number per contact via pad structure. The said interlocking grid structure 6, formed in a pad via contact region forms in three dimensions, a "grid", group or an array of interlocking structures ("islands").

Listing of Claims:

Claims 1-33 (canceled)

34. (currently amended) A bond pad structure, comprising:

a semiconductor substrate;

comprising interlocking grid structures, formed over said semiconductor substrate;

a passivating layer forms ~~formed over~~ said, interlocking grid structures, having multiple openings to said interlocking grid structures;

a barrier layer formed of tantalum nitride over said passivating layer and in said openings;

a conducting pad formed over said interlocking grid structures and over said barrier layer, whereby an upper surface of said conductive pad provides improved adhesion for subsequently formed *bonds*.

35. (previously amended) The bond pad structure of Claim 34, wherein said conductive bond pad is formed of copper. ~~or Aluminum~~

36. (original) The bond pad structure of Claim 34, wherein said passivating layer is selected from the

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-33. (Cancelled)

34. (Not entered)

35. (Previously presented) The bond pad structure of Claim 34, wherein said conductive pad is formed of copper.

36. (Original) The bond pad structure of claim 34, wherein said passivating layer is selected from the group consisting of silicon oxide, silicon nitride and polyimide.

37. (Previously presented) The bond pad structure of Claim 34, wherein said bond pad forms an interlocking grid array in the bond pad via contact region, which is approximately 100 by 100 microns square and the size of the island structures are from about 10 to 25 microns in width, approximately 4 microns in height, and from about 4 to 10 in number, of interlocking grid structures, increasing surface area for improved adhesion.

38. (Previously presented) The bond pad structure of Claim 34, wherein said conductive bond pad is formed of aluminum.

39. (Cancelled)

40. (New) A bond pad structure for a semiconductor device, the structure comprising:
an insulator layer adjacent to a semiconductor substrate;

a metal wiring layer adjacent to the insulator layer;

a passivation layer adjacent to the metal wiring layer, wherein at least a portion of the passivation layer is configured to provide a plurality of island structures separated by spaces that expose a portion of the underlying metal wiring layer;

a metal barrier layer covering the passivation layer and the exposed portions of the metal wiring layer, wherein the metal barrier layer conforms to a shape provided by the island structures; and

a metal pad layer covering the metal barrier layer.

41. (New) The bond pad structure of claim 40 wherein the metal barrier layer is substantially the same thickness throughout the bond pad structure.

42. (New) The bond pad structure of claim 40 wherein the metal pad layer fills the spaces and rises above the island structures.

43. (New) The bond pad structure of claim 40 wherein the passivation layer is selected from the group consisting of silicon oxide, silicon nitride and polyimide.

44. (New) The bond pad structure of claim 40 wherein the metal pad layer is formed of aluminum.

45. (New) The bond pad structure of claim 40 wherein the metal barrier layer is formed of tantalum nitride.

46. (New) A bond pad structure for a semiconductor device, the structure comprising:

a first metal layer overlaying an insulator layer;

a plurality of vertical structures extending from the first metal layer upward and separated from each other by exposed portions of the first metal layer, wherein the vertical structures are formed from a passivating material; and

a second metal layer covering the vertical structures and the exposed portions of the first metal layer, wherein the second metal layer substantially conforms to a non-planer shape provided by the vertical structures.

47. (New) The bond pad structure of claim 46 further comprising a third metal layer covering the second metal layer, wherein the third metal layer surrounds and rises above each of the vertical structures.

48. (New) The bond pad structure of claim 46 wherein the second metal layer is substantially the same thickness over both the vertical structures and the exposed portions of the first metal layer.